REMARKS/ARGUMENTS

Applicants received the Office Action dated January 20, 2004, in which the Examiner: (1) objected to Figures 1-3; (2) objected to the specification for various informalities; (3) objected to claim 1 for an informality; (4) rejected claims 1-4, 9-12, 17-19, 24-28, and 33-35 as anticipated by Carr ("Compiler Optimizations for Improving Data Locality"); and (5) rejected claims 5-8, 13-16, 20-23, and 29-32 as obvious over a combination of Carr and Mahadevan (U.S. Patent No. 5,797,013). In this Response, Applicants amend the specification and claims 1, 9, 17, 24-26, 34, and 35. Based on the arguments and amendments contained herein, Applicants believe all claims to be in condition for allowance. Accordingly, Applicants respectfully request reconsideration and allowance of the pending claims.

I. DISCLOSURE OBJECTIONS

The Examiner objected to Figures 1-3 as allegedly illustrating prior art. Applicants respectfully traverse this objection for the following reasons. Figure 1 illustrates a computer system that may be used to implement embodiments of the invention. Figure 2 illustrates a compilation procedure performed by the computer of Figure 1 that may be used to incorporate embodiments of the invention, namely the compiler of claim 26. Figure 3 illustrates one embodiment of a portion of the computer system of Figure 1. As such, Figures 1-3 are used to illustrate embodiments of the invention.

The Examiner also objected to the specification for various informalities. Applicants amend the specification to correct these various informalities. In addition, Applicants amend the specification on page 12, line 14 to replace the phrase "loop disibution" with "loop distribution."

II. CLAIM REJECTIONS

Amended claim 1 recites a method that comprises, among other limitations, "reducing cache thrashing by distributing the vector memory references into a plurality of detail loops, wherein the vector memory references that have circular dependencies th rebetween are included in a common detail

loop, and wherein the detail loops are ordered according to the unidirectional dependencies between the memory references." The art of record does not teach or even suggest the above-cited limitation. More specifically, Carr teaches a system that uses "loop distribution to indirectly improve reuse by enabling loop permutation on a nest that is not permutable." Page 256, col. L, lines 52-54. The effect of the loop distribution is to "improve data locality." Abstract, lines 5-6. Carr does not teach or suggest the desirability to reduce cache thrashing, much less reducing cache thrashing by distributing the vector memory references into a plurality of detail loops, as required by claim 1. As can be appreciated by one of ordinary skill in the art, improving data locality is different from reducing cache thrashing. Improving data locality refers to increasing the performance of a memory by storing related elements of data in close proximity of each other (*e.g.*, storing elements of a loop in the same cache line). By contrast, reducing cache thrashing refers to minimizing or eliminating the eviction of needed data from the cache. Although not used to reject claim 1, Mahadevan is similarly deficient. Thus, the art of record does not anticipate nor render obvious the invention of claim 1 and dependent claims 2-8

Amended claim 9 is directed to a method that comprises, among other features, "reducing cache thrashing by distributing the vector memory references into a plurality of detail loops, wherein the vector memory references that have dependencies therebetween are included in a common detail loop." As explained above regarding claim 1, Carr and Mahadevan do not teach or even suggest reducing cache thrashing by loop distribution. Thus, the art of record does not anticipate nor render obvious the invention of claim 9 and dependent claims 10-16.

Amended claim 17 is directed to a method that comprises, among other features, "reducing cache thrashing by distributing the vector memory references into a plurality of detail loops in response to cache behavior and the dependencies between the vector memory references in the loop." As explained above regarding claim 1, Carr and Mahadevan do not teach or even suggest reducing cache thrashing by loop distribution. Thus, the art of record does not anticipate nor render obvious the invention of claim 17 and dependent claims 18-23.

Amended claim 24 is directed to a method that comprises, among other features, "reducing cache thrashing by distributing the vector memory references into a plurality of detail loops, wherein the vector memory references that have circular dependencies therebetween are included in a common detail loop." As explained above regarding claim 1, Carr and Mahadevan do not teach or even suggest reducing cache thrashing by loop distribution. Thus, the art of record does not anticipate nor render obvious the invention of claim 24.

Amended claim 25 is directed to a program storage medium that comprises, among other features, "reducing cache thrashing by distributing the vector memory references into a plurality of detail loops, wherein the vector memory references that have circular dependencies therebetween are included in a common detail loop." As explained above regarding claim 1, Carr and Mahadevan do not teach or even suggest reducing cache thrashing by loop distribution. Thus, the art of record does not anticipate nor render obvious the invention of claim 25.

Amended claim 26 is directed to a compiler that comprises, among other features, "means for reducing cache thrashing by distributing the vector memory references into a plurality of detail loops, wherein the vector memory references that have circular dependencies therebetween are included in a common detail loop, and wherein the detail loops are ordered according to the unidirectional dependencies between the memory references." As explained above regarding claim 1, Carr and Mahadevan do not teach or even suggest reducing cache

thrashing by loop distribution. Thus, the art of record does not anticipate nor render obvious the invention of claim 26 and dependent claims 27-32.

Independent claim 33 is directed to a method for reducing the likelihood of cache thrashing by software to be executed on a computer system that comprises, among other features, "modifying the identified portion of the software to reduce the likelihood of cache thrashing." As explained above regarding claim 1, Carr and Mahadevan do not teach or even suggest reducing cache thrashing by loop distribution. Thus, the art of record does not anticipate nor render obvious the invention of claim 33 and dependent claim 34.

Amended claim 35 is directed to a method that comprises, among other features, "reducing cache thrashing by distributing at least a portion of the first portion of the memory references into distinct loops, and placing at least the second portion of the memory references into the distinct loops." As explained above regarding claim 1, Carr and Mahadevan do not teach or even suggest reducing cache thrashing by loop distribution. Thus, the art of record does not anticipate nor render obvious the invention of claim 35.

Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may

be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Respectfully submitted,

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